

Evaluation of Industrial Surface Mount Plastic Encapsulated Microcircuits for Military Avionics Applications

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Abstract

This paper will focus on thermal cycling and moisture susceptibility of plastic encapsulated microcircuits for use in military avionics digital processing modules. Today's avionics designs often use low profile Standard Electronics Module-Size E (SEM-E) modules, which preclude the use of through-hole (DIP) microcircuit technology. This fact pushes the design selection of microcircuits to surface-mount, thin, small outline packages (TSOPs) and small outline J-leaded (SOJ) packages.

For this study, 1248 plastic surface-mounted (SMT) integrated circuits (ICs), representing 19 different part types from 9 different manufacturers, were reflow solder-attached to 69 high temperature BT epoxy circuit boards on an automotive electronics assembly line. **Figure 1.** is diagram of a fully assembled test board prior to any environmental testing. The test boards were then subjected to a series of accelerated tests as shown in **Figure 2.**, for the purpose of evaluating thermal cycling and moisture susceptibility of the plastic SMT ICs.

The final test results are summarized and the failure analysis results for devices not passing the test are presented, with a discussion of device failure mechanisms.

Finally, a reliability assessment is made for each of the test environments based on calculated acceleration factors, using currently accepted acceleration models^[1]. The acceleration factors and levels of stress testing are presented, as well as the methods for extrapolating the accelerated test conditions to typical military avionics application conditions.

I. Introduction

Surface-mount plastic encapsulated microcircuits (PEMs) are used in commercial and industrial electronics designs, primarily for their cost and size advantage. They are easily adaptable to automated assembly operations. As a result of their application in high commercial communications systems and automotive electronics, many improvements have been made in the package

molding compounds to better withstand the environmental extremes of temperature and moisture.

Today's military avionics designs, with requirements for high reliability, reduced size and low weight, are an obvious choice to take advantage of these improvements in the industrial microcircuit technology base, wherever possible.

Table I. shows the nineteen different microcircuits that were chosen as candidates for the thermal and moisture accelerated testing evaluation. The commercially available devices selected had to meet the form, fit and function requirements of current military avionics module designs. All the devices were surface-mount plastic encapsulated packages with either gull-wing leads or J-leads. Lead pitches ranged from .5 mm (.020 inches) to 1.25 mm (.050 inches) and the overall package heights were no greater than 3.8 millimeters (.150 inches).

II. Manufacture of Test Boards

A high temperature (180°C rated) BT epoxy circuit board material was selected as the test carrier for the microcircuits. The primary purpose of mounting the devices on circuit boards was two-fold. (1) The exposure the devices saw during the solder reflow operation provided a preconditioning that was representative of actual manufacturing conditions. (2) The design of the boards was such that all devices could be electrically probe tested from the backside of each board by means of a bed-of-nails test fixture at a GENRAD test station.

Prior to the solder reflow operation the devices were subjected to a 24 hour bake at 40°C, to minimize the risk of package rupture due to rapid moisture expansion during the reflow temperature exposure. This is not standard procedure for a high volume automotive electronics production line. Moisture sensitive components are normally received in protective packaging from the part manufacturer. The level of production is usually such that the components are exposed to room ambient conditions for only a short period of time prior to actual reflow attach. However, the relatively small quantity of components selected for this test had been removed from their packaging for an extended period of time and the actual levels of moisture absorption into the microcircuit packages was unknown. Thus, all the microcircuits were subjected to the moisture bake-out prior to the solder reflow operation.

The resulting solder reflow operation for the 69 test boards was performed on an automated flex line typically used to assemble automotive electronics circuit boards.

The critical parameters of the solder reflow profile used for the test boards were:

- 1) The maximum channel temperature was +220°C
- 2) The preheat rise rate (maximum slope) was 1.9°C per second.
- 3) The liquidus time (time above +183°C) was 79 ±3 seconds
- 4) The soak time (time at +150±10°C) was 158±10 seconds

Following reflow component attach the circuit boards were visually examined for defects and then electrically tested at room ambient (+25°±3C) on a GENRAD 2284 in-circuit test station.

The tested good boards were then segregated into three groups for conformal coating:

- 1) 28 - coated with silicone
- 2) 26 - coated with parylene
- 3) 15 - not coated

The purpose of incorporating conformal coatings in the experiment was to evaluate their effectiveness in minimizing package lead corrosion.

The back (non-component) side of the boards were left uncoated to allow the bed-of-nails test head at the GENRAD test station to make contact with the device test points on the bottom of the boards.

III. Experimental Procedure

A. Extended Burn-in

68 of the 69 boards were subjected to a schedule of extended burn-in at +125°C, with the goal of achieving 100 - 200 hours. While the accumulated device-hours of the burn-in was not sufficient to establish a meaningful failure rate, it did provide an additional level of confidence of reduced infant mortality.

B. Temperature cycling

63 of the 69 boards were then temperature cycled from -65°C to +150°C per JEDEC STD 22-A104. The boards were loaded horizontally into a holding rack as shown in **Figure 3.**, which was subsequently loaded into a Ransco Model 7103-1 temperature cycling test chamber equipped with a vertical elevator to automatically transfer the parts from one temperature extreme to the other. The time at each temperature extreme (dwell) was 12 minutes. The actual transfer time was less than 1 minute.

-65°C was achieved by liquid nitrogen purge-boost to ensure that the holding rack and test boards would reach the low temperature extreme within the required 15 minutes. In addition to the chamber thermal probes, a thermocouple was attached to a test board located on an inner row of the rack. The thermocouple wire was carefully routed along the edge of the chamber elevator and outside, to a digital monitor, with sufficient slack to assure that it would not be torn loose during the actual physical transfer.

Following the completion of 518 cycles the boards were removed and visually examined for evidence of component damage (i.e. package delamination or cracking), prior to electrical endpoint testing.

C. Autoclave

Autoclave test was performed on 50 boards using the Triotech / Express Test H6000X test chamber. The testing was performed at temperature of +121°C, 15psig, 100%RH for 96 hours per JEDEC STD 22-A102. All the boards were loaded vertically into a stainless steel rack that fit in the autoclave chamber. A pre-programmed test sequence was then initiated which automatically ramped the chamber up to the required test conditions and proceeded to run the 4-day test. At completion, the chamber ramped down to room ambient conditions.

The boards were removed and the components were visually examined for evidence of package damage or lead corrosion. The electrical endpoint testing was repeated at the GENRAD test station.

D. Highly Accelerated Stress Test (HAST)

HAST testing was performed on 55 boards using the same Triotech / Express Test H6000X test chamber reprogrammed for +125°C, 85%RH, 240 hours duration using JEDEC STD 22-A110 as the basis for performing the test.

Figure 4. shows the biasing configuration of the 55 boards subjected to HAST testing. Since each board had a mix of digital and analog components, it was necessary to run five bias lines to each board (+5vdc, digital ground, +15vdc, -15vdc, and analog ground).

The 55 boards were arranged in the chamber in three layers, bussed in parallel and tied together at terminal strips on the back of the power supplies external to the HAST chamber. The total +5vdc, -15vdc and +15vdc currents were continuously monitored at the three external supplies (one for each voltage). Individual power lines to each of the three layers of boards were arranged to permit daily current probe measurements.

When the boards had all been properly configured and the current readings were baselined, the HAST test program was initiated. The chamber ramped up to the required +125°C, 85%RH. Chamber pressure ramped up to 15 psig in order to insure a non-condensing humidity environment. The testing proceeded until 168 hours (7 days) of testing had been accumulated. At that time the chamber was ramped down in order to perform intermediate current readouts on each board. 5 of the boards had significant current reductions (5 to 10 mA), and were removed from the test population for further analysis.

Testing was resumed on the remaining 50 boards until a total exposure time of 240 hours had been accumulated, at which time the chamber automatically ramped down to room ambient conditions and the boards were removed.

The components were visually examined for evidence of package damage and lead corrosion. The electrical endpoint testing was performed at the GENRAD test station.

Parametric GENRAD Testing

Each of the 69 test boards were probed tested on the bed-of-nails test fixture connected to a GENRAD 2284 in circuit test station. The test program was structured to perform an initial bias circuit integrity check (power, ground, resistance) prior to applying power to the microcircuits. The 19 microcircuits on each board were then functionally tested in sequence. Device failures were identified and the results were printed out at the conclusion of the board test.

IV. Test Results

Table II summarizes the overall test results by board quantities and the number of microcircuits tested for each of the environmental tests conducted.

A. Extended Burn-in Test Results

Table III. shows the summary of the accumulated burn-in test hours for all the boards. While 62 of the 69 boards saw between 100 and 200 hours of accumulated burn-in, the first 4 pilot boards (with no conformal coating) entered the burn-in test 16 days before the remainder of the boards had completed their parylene or silicone conformal coating and thus accumulated 525 hours each. The last 2 boards completed only saw 40 hours of burn-in before testing was terminated.

4 devices were verified to be failures at the conclusion of the burn-in testing. Three of them were (U19) comparators on the pilot boards that saw 526 hours of burn-in. The other device was a 20 bit buffer circuit (U15) which was also on one of the pilot boards. These 4 devices were submitted for failure analysis

B. Temperature Cycling Test Results

The temperature cycle test was performed on 63 boards which successfully passed the GENRAD functional testing. The 6 boards not subjected to this test included the original control board (3C), 23A designated for salt fog testing and 4 boards held back for circuit board rework.

Upon completion of the 518 cycles, the boards were removed from the chamber and visually examined. All the microcircuits had remained attached with no apparent external package or lead damage. The two predominant visual conditions were (1) a distinct granularity to the solder used to attach the components to the circuit boards and (2) crazing and lifting of the conformal coating on the boards coated with parylene.

The boards were then subjected to GENRAD parametric testing. Many of the boards failed this test as a result of fractured ceramic bias resistor networks (RN1- RN12 in Figure 1), that were not rated to survive the repeated temperature cycle extremes. The failed resistors were replaced and the boards were retested. As a result of the rework, 50 of the previously failed boards now

passed. However, a quantity of boards (13) still remained that did not pass, and these boards were set aside for further investigation.

The follow-up investigation of the 13 failed boards revealed that temperature cycling had caused fractures in circuit board through-hole vias that were used as test points for the GENRAD functional testing. Consequently, electrical continuity had been broken between the backside probe pad and the microcircuit on the topside of the board.

In any case, none of the microcircuits were verified to have failed as result of the temperature cycle testing.

C. Autoclave Test Results

The 50 boards subjected to autoclave exhibited circuit trace corrosion (predominantly on the uncoated boards). The boards coated with silicone and parylene, exhibited a lesser degree of corrosion on traces under the conformal coating. The parylene appeared to be a better barrier than the silicone, except in localized areas where the parylene had previously crazed in the temperature cycle test.

Corrosion was also in evidence on the microcircuit package leads. Here again, it was predominantly in evidence on the uncoated boards. The greatest concentration of corrosion appeared at the ends of the leads where trimming had exposed unplated base metal, and at the flex radii of the formed leads.

In no case did the corrosion result in package lead separation, degradation, or shorting such that the functionality of the devices was affected. However, the moisture environment of autoclave did cause additional failures of circuit board vias and resistor bias networks. Intermittent fractures of board vias and ceramic resistors, as a result of the earlier temperature cycling, were now open as a result of the moisture corrosion effects of Autoclave.

Many of the boards were repaired by soldering jumper wires through the via holes to re-establish continuity.

One microcircuit device was verified to be a failure at the conclusion of the autoclave test. A quad operational amplifier (U7) failed one of its outputs and was submitted for failure analysis.

D. HAST Test Results

As a baseline for the HAST test, all the boards were biased prior to the test and the currents recorded. Following the interim test after 168 hours of HAST, 5 boards exhibited a current reduction or fluctuating current and were consequently held out from the remaining 72 hours of HAST. Subsequent evaluation of the boards and components revealed these problems were related to the degradation of the boards (bad vias) and not the result of actual component failures.

At the completion of the 240 hours of HAST environment, all the currents being monitored remained stable (see **Table IV**). Following the chamber ramp-down, the boards were powered down and removed from the chamber.

Further evidence of circuit board trace and component lead frame corrosion were seen. Still, all leads on all devices remained intact and all devices remained attached to the boards.

E. Final Functional Test Results

34 of the original 69 boards passed final parametric testing on the GENRAD with no microcircuit failures. The 35 remaining boards had 91 microcircuits that did not pass GENRAD parametric testing. A decision was made to remove these microcircuits from the remaining failed boards and test each microcircuit individually. The intent was to eliminate any variables associated with previous circuit board failures (open vias, resistors, fractured solder, etc.).

To accomplish this task, some devices (11) were bench tested in-house, where test fixtures were available and the remaining (80) devices were sent to the original manufacturers for functional testing.

At the conclusion of all the microcircuit testing (both on and off the boards), 7 confirmed microcircuit failures were identified. **Table V** summarizes the final test results for the individually tested microcircuits.

V. Failure Analysis

A. Failure Definition

Prior to initiating the test plan it was necessary to define what would constitute a failure. This was essential in determining which microcircuits would require analysis and which would not. As a baseline, the following failure criteria were used:

- 1). Test failures were devices not passing the parametric (GENRAD) testing or the device manufacturer's testing.
- 2). Any device that visually appeared to be physically damaged (i.e. cracked package, damaged leads) was also considered to be a failed device. (Physically damaged devices that were not test failures could continue through testing and be closely tracked for evidence of further degradation).
- 3). If the cause of the failure was due to mishandling or improper testing, the failure was discounted, but reported as part of the data submission.
- 4). All failures were documented by device and board serial number.
- 5). Board-related or solder-related failures were repaired in order to continue device testing.
- 6). Verified, device test failures (not solder or PWB related) were to be removed for failure analysis.

B. The failure analysis plan

Each of the 7 devices verified to be failures by the above criteria were submitted for analysis to determine the failure mechanism(s). **Figure 5** describes the approach taken for the failure analysis.

C. Analysis Results

Table VI. summarizes the test stresses seen by the boards that exhibited component failures. These failures were submitted to ERS Inc. for failure analysis^[2]. Components from the additional boards listed (2b and 9a) were studied as a comparison to the failed parts.

Electrical characterization of the devices was performed at TRW and, in some cases, by the part manufacturer. The electrical identification of the failure mode, failure site, and point in the testing at which the failure occurred provided important clues as to the potential failure mechanisms and helped govern the subsequent failure analysis, which was conducted at ERS Inc.

Parts failing after extended burn-in

Two (U19) comparators (from boards 7c and 13b) failed after 525 hours of burn-in at +125°C, when outputs Q (pin7) and Q_{not} (pin8) remained stuck at levels

independent of the inputs IN+ (pin2) and IN- (pin3). The most probable failure mode was an open circuit at the input pins of the comparators.

There was no visual evidence of any through-package cracking. Acoustic microscopy was used to look for package delaminations at the die surface, as these could introduce additional stresses on the die metallization and wirebonds. No delamination or internal cracking was observed on these parts. X-radiography showed no evidence of broken, shorted, or lifted bondwires.

One of the comparators (from board 7c) was cross-sectioned through the bondwires on die bond pads 2 and 3. An excessive amount of intermetallic growth was found on the bond pads, when compared with a “good” bond pad that was not exposed to the burn-in stress. The excessive thickness of the intermetallic layer on the failed bond pad is illustrated in **Figure 6**, which also shows the uneven insular nature of the intermetallics and the voiding in and around the intermetallic layer. Both of these conditions can contribute to a weakening of the bond and an eventual open circuit. Given the lack of any other physical or electrical damage, the excessive intermetallic condition at the wirebond-bond pad interface was the most probable failure mechanism.

The other comparator (from board 13b) was chemically decapsulated and the top view did not show the emergence of intermetallics from under the ball bonds and a subsequent average bond shear force of 152g was not indicative of excessive intermetallics. However, an examination of the die metallization trace revealed hillock and void formation, mostly seen at the ends and corners of metallization traces. This condition was primarily due to either thermally induced stress relief or current density driven electromigration.

A third comparator (from board 5c) failed in burn-in by a short circuit between pins 4 and 6 after 525 hours at +125°C. It was unlikely that this failure was due to intermetallic formation at the bondwire-bond pad interface because it failed as a short circuit rather than an open.

Here again, the external examination and non-destructive acoustic and X-ray scanning revealed no evidence of cracks or delaminations in the plastic encapsulant material, and no lifted, broken, or shorted bondwires.

Chemical decapsulation revealed evidence of hillock formations in the die metallization, which could lead to a short circuit in the traces connecting bond pads. However, a more interesting finding was the presence of a number of whisker-like growths at the bond pads, as shown in **Figure 7**. While it was initially thought to be intermetallic growth, subsequent energy dispersive spectroscopic (EDS) analysis revealed that it was silver migration. This metal migration can cause short circuit failure if it links to pads or metal traces. In this case it was not observed to link pads 4 and 6, however, it is often the case that

when a failure occurs by this mechanism, the dendritic growth is consumed by the heat dissipated by the short circuit and the evidence is lost.

A 20 bit buffer (U15) from board 7c also failed immediately after burn-in. Here again, there was no evidence of package cracking or delamination and no broken, lifted, or shorted bondwires. Decapsulation did reveal evidence of excessive intermetallic formations emerging from under the ball bonds as shown in **Figure 8**. EDS analysis determined the formations to be composed of gold and aluminum. In addition to this, lower than usual average ball bond shear strength of 100g was observed.

Parts failing after autoclave

A fourth (U19) comparator (from board 12b) failed after autoclave testing. Again the failure mode was that the outputs Q (pin7) and Q_{not} (pin8) remained stuck at levels independent of the inputs IN+ (pin2) and IN- (pin3). Because this failure mode was similar to that seen in parts which failed from burn-in stress alone, it was postulated that, even though this device was exposed to humidity and temperature in autoclave, it probably also failed due to an open circuit at the input pins due to excessive intermetallic formation at the bond pads. The fact that the part did not fail immediately after burn-in, as was the case with the other comparators, was attributed to the fact that it was exposed to only 159 hours of burn-in instead of 525 hours. Destructive physical analysis did in fact reveal the presence of excessive intermetallic formation. Even more interesting, however, was the presence of the large amount of silver dendritic, as shown in **Figure 9**. This may be an alternate reason for the observed failure. The reason for more widespread growth in this sample over the other comparators analyzed is the exposure of this sample to moisture during autoclave.

The failure mode for the quad op amp (U7 from board 21a) was that output B stayed at 4 volts regardless of the input, indicating a failure at the C output, pin 10. Because of the failure mode and the elevated temperature and humidity test stresses encountered in autoclave, this device was examined for evidence of corrosive failure. This included acoustic microscopy for evidence of delamination and cracking that could provide a path for moisture ingress to the surface of the die. A mechanical decapsulation was performed on this part to minimize the loss of corrosion artifacts that could occur with a chemical method of decapsulation.

The scanning acoustic microscopy revealed the presence of delamination on the top of the die as shown in **Figure 10**. X-radiography showed no evidence of broken, shorted, or lifted bond wires.

The failed op amp was mechanically decapsulated along with two other op amps used as controls. The first control (from board 2b) had also been exposed to

autoclave, but exhibited no delaminations. The second control (from board 21c) had not been exposed to autoclave. The failed sample as shown in **Figure 11** had significantly more corrosion at the bond pads than either of the two controls. Also, the ball bonds were so weakened by the corrosion that most were pulled off the failed sample during the mechanical decapsulation, but most of the bonds remained on the control samples during the decapsulation. The relative bond strength results were quantified by the results of ball shear testing which indicated that the average bond shear strength for the failed sample was 65 gram force while that for the control samples was in the 97 to 101 gram force range.

Perhaps the most fascinating result was the fact that the op amp with no delamination that was exposed to autoclave exhibited equal bond strength to the one which not exposed to autoclave at all. This supports the premise that parts with no package delamination are less likely to corrode than parts with delaminations.

Parametric test failure

Finally, one 20 bit buffer (U15 from board 5a) showed up as a parametric test failure after autoclave testing. It was not clear that this tolerance-related issue was indicative of degradation, since the device was not tested to the manufacturer's detailed test specification, initially. Nevertheless, an analysis was performed to examine the condition of the device.

There was a limited amount of lead corrosion at the trimmed ends of the leads and at the interface to the package due to exposed copper and absence of plating at these locations. There was no visual evidence of package cracking. Acoustic microscopy and X-ray yielded no evidence of delamination or bondwire failures.

The chemical decapsulation and E-SEM revealed small spikes of Al-Au intermetallic growth emerging from under the ball bonds as shown in **Figure 12**. Subsequent ball shear testing revealed that the bond had acceptable but somewhat weakened average bond strength of 101 gram force. The intermetallic formation could eventually be responsible for changes in contact resistance leading to parametric shifts.

VI. Discussion

A. The Military Avionics Using Environment

This environment is typically characterized by daily, time-limited, power-on operation over an extended lifetime (i.e. 20yrs, 12,000 op hours).

It is imperative to understand what a baseline application environment is prior to imposing accelerated tests on microcircuits. Under-acceleration may not adequately stress the devices to reveal the potential failures that could occur during normal life, whereas over-acceleration can result in creating failures that would not typically occur in the actual life of the product.

Typical characteristics of the military avionics environment include:

Operational profile:

- * 8000 flight hours/20 years = 400 flight hours/ year avg.
- * 4800 ground op hours/20 years = 240 ground op hours /year avg.
- * Total operating hours/year = 640 avg.
- * 640 op hours/8760 hours/year = 7.3% op time vs. 93% non-op time

Thermal Exposures:

- * Diurnal (unbiased), -54°C to +58°C - 93% of the time (1490 cycles)
- * Ground op (biased), -40°C to +85°C - 2.7% of the time (2668 cycles)
- * Flight (biased), -40°C to +74°C - 4.6% of the time (5334 flights)

Humidity:

- * Typically 50% of the time is above 80%RH

B. Discussion: Extended Burn-in

Combining all the burn-in test hours shown in **Table III.**, the maximum accumulated device-hours per device type is about 10,700 device-hours. Even if no failures had been observed, a calculated failure rate, using the Arrhenius equation for a 60% confidence level, +75°C use temperature and an activation energy of 0.7eV, would translate to 2.1%/1000hours or 21,000 FITs. Clearly, in order to arrive at a meaningful life prediction, many more device test hours would need to be accumulated. However, the test results for this time/temperature exposure are an indication of reduced infant mortality, for those device types exhibiting a zero failure rate.

C. Discussion: Temperature Cycling

Functional test results indicated there were no microcircuit failures as a result of the temperature cycle testing. However, there were three circuit board-level anomalies that occurred as a result of the temperature cycle test.

1) Conformal coating

Many of the boards conformally coated with parylene experienced a crazing and, in some cases actual blistering of the parylene coating following the exposure to the temperature cycling. The supplier of the coating reported that the thermal endurance of the coating is established by using a weight-loss factor during an accelerated temperature test, rather than actual property changes of the coating. Supplier accelerated test data showed that measurable weight loss can occur at +150°C after approximately 100 hours of exposure.

Since the boards in question saw 10-12 minutes of +150°C exposure during each of the 518 cycles, the total accumulated exposure closely approximates the 100 hour limit predicted by the coating supplier. In addition, the supplier also indicated that, as measurable weight loss begins, some property change has already occurred. Thus, the supplier recommends a 10 -15°C reduction in the predicted maximum exposure temperatures. This would bring the maximum recommended temperature down to about +135°C for a 100 hour exposure.

The temperature cycling test environment was intended to accelerate any microcircuit failure mechanisms based on a reasonable test duration and temperature. However, the parylene coating was thermally over-accelerated. Since the actual operating conditions in the intended environment will never see this accelerated temperature level, the recommended solution would be to evaluate the coating using a reduced (but still accelerated) high temperature

(i.e. +130°C) for the cycling test with an extended number of test cycles. This in fact, was planned into a follow-on series of tests.

Bias resistors

Another problem experienced as a result of the temperature cycle test was the damage caused to ceramic network resistors. These components provided bias for the microcircuits during the functional testing. They were not being evaluated as part of the test plan. In any case, the selection of these particular components was inappropriate since the rated operating temperature of the resistors was exceeded and, in addition, the thermal characteristics (CTE) of the resistors were not suitably matched to the thermal characteristics of BT epoxy circuit board material.

The fractures occurred predominantly at the interface of the soldered coated pads (resistor terminations) to the body of the ceramic material.

Replacement of the damaged resistors was accomplished to allow the testing to continue.

Printed Circuit Board Vias

Additional circuit board failures were experienced in temperature cycling as a result of expansion and contraction of the through-hole vias. Failures occurred when the inner barrel of the via separated from the trace pad on either the top or the bottom of the circuit board, causing an open electrical path from the microcircuit on the top of the board to the test point on the bottom of the board.

Many of the open vias were repaired by soldering jumper wires through the hole to re-establish electrical continuity. This was not possible for vias that existed directly under components. In these cases, the components were removed for electrical test verification.

Temperature cycle reliability assessment

The reliability assessment for temperature cycling is based on the Coffin-Manson relationship. Its applicability for plastic encapsulated microcircuits relates to the stresses caused by thermal expansion mismatches among the different packaging, die, and leadframe materials used. Even though moisture is not a factor in the Coffin-Manson equation, any resultant stress cracking and delamination caused by thermal mismatches during the thermal cycling can provide a path for moisture and contaminant ingress to the die surface of the microcircuit being tested.

The Coffin-Manson equation, as it applies to temperature cycling of PEMs below 10,000 cycles (low cycle fatigue) is:

$$(1) \quad \Delta T N_f^b = C$$

where:

ΔT = the temperature cycle range

N_f = the number of cycles to failure

C = material constant

b = material fatigue exponent

The acceleration factor that relates the use conditions to the accelerated test conditions is calculated by:

$$(2) \quad A.F. = N_{f \text{ use}} / N_{f \text{ test}} = (\Delta T_{\text{test}} / \Delta T_{\text{use}})^{1/b}$$

This assumes that the material fatigue exponent, b , does not vary being the test and use conditions. The currently accepted value for the acceleration factor exponent, $1/b$, ranges between 4 and 7, with the more conservative value being 4.

If we take the accelerated test conditions used for testing the boards in this experiment:

-65°C to +150°C for 518 cycles

and the typical thermal cycle conditions for a circuit board in the using avionics environment:

Non-operating (diurnal): 1490 cycles, (-54°C to +58°C)

Ground operations: 2668 cycles, (-40°C to +85°C)

Flight operations: 5334 flights, (-40°C to +74°C)

we can calculate an acceleration factor using equation (2) and the flight operations using conditions, which are the predominant thermal exposure in terms of number of cycles and temperature range.

$$A.F. = (215^{\circ}\text{C}/114^{\circ}\text{C})^4 = 12.7$$

The experiment performed is based on the assumption that all devices would fail at 519 cycles, with zero failures at 518 cycles. Thus, with an acceleration factor of 12.7 the predicted life cycles is $(12.7) * (518) = 6578$ cycles.

Now if the typical avionics flight environment is 5334 flights / 20 yrs, the above calculation equates to:

$$\begin{aligned} & (6578 \text{ cycles/lifetime}) / (5334 \text{ flights cycles/lifetime}) * (20\text{yrs}) \\ & = \mathbf{24.6 \text{ yrs}} \end{aligned}$$

D. Discussion: Autoclave

Some consider the autoclave to be a non-powered “pressure cooker” test to evaluate the moisture resistance of a microcircuit. This is accomplished by accelerating the moisture penetration through the package material to the surface of the microcircuit die, through pressure and temperature in a 100% RH environment.

Since it is a non-powered test the major failure mechanism; corrosion, is galvanic in nature, rather than electrolytic. This type of corrosion is additionally accelerated through external ionic contaminants, ionic contaminants in the package encapsulant material and phosphorus in the die passivation.

Autoclave reliability assessment

The assessment of reliability for autoclave is based on Peck’s model. Even though this model does not specifically address ionic contamination, it does address the acceleration factors of moisture and temperature, which promote the corrosion in the presence of ionic contaminants.

Calculation of the acceleration factor based on Peck’s model states:

$$(3) \quad A.F. = (RH_{\text{use}})^n \exp(Ea/K*T_{\text{use}}) / (RH_{\text{test}})^n \exp(Ea/K*T_{\text{test}})$$

where A.F. = the acceleration factor of the “test” environment over the anticipated “use” environment.

$$K = 8.631 \times 10^5 \text{ eV/K}$$

$$E_a = 0.9 \text{ eV}, -n = 3.0$$

In order to predict a device lifetime for a military avionics environment, we select the conservative ambient conditions of:

1) 41°C and 88%RH; a combination of temperature and humidity that reflects the diurnal extremes for the 1% worldwide hot /high absolute humidity region.

2) 40°C and 73%RH; a combination of temperature and humidity that reflects the average of the diurnal extremes for the five 1% worldwide regions.

Condition 1) represents the worse case region of the five regions described in MIL-STD-210 for high temperature and humidity. If we consider condition 1) to represent the military avionics environment previously discussed where 50% of the design life will be above 80%RH and condition 2) to represent the remainder of time below 80%RH, then the acceleration factors, based on the autoclave test conditions used of 121°C, 100%RH for 96 hours are:

using equation (3):

for condition 1):

$$\text{A.F.} = (0.88)^3 \exp(E_a/K*314) / (1.00)^3 \exp(E_a/K*394) = 1244$$

for condition 2):

$$\text{A.F.} = (0.73)^3 \exp(E_a/K*313) / (1.00)^3 \exp(E_a/K*394) = 2423$$

For the 96 hours of accelerated testing performed, these acceleration factors equate to 119,424 and 232,608 hours of predicted life, respectively. If we take condition 1) by itself, this translates to an expected life of:

$$(119,424 \text{ hours} / 8760 \text{ hours/yr}) = 13.6 \text{ years}$$

However, since we assumed condition 1) to be present only 50% of the time, it must be factored with condition 2) existing for the other 50% of the time.

Condition 2) by itself would translate to an expected life of:

$$(232,608 \text{ hours} / 8760 \text{ hours/yr}) = 26.5 \text{ years}$$

Therefore a reasonable estimate of the expected life would be an average of the two lifetimes calculated above, or approximately **20 years**.

E. Discussion: HAST

The highly accelerated stress testing (HAST) performed on the test boards of this experiment stressed the devices in an elevated temperature and non-condensing humidity environment, under nominally biased conditions. The purpose was to accelerate failures at the microcircuit die level caused by electrolytic corrosion, increased intermetallic growth, and reduction of isolation resistances, as a result of potential moisture/contaminant ingress through the packaging material to the biased circuitry.

It was decided to maintain a continuous bias during the test, as the majority of the devices were at or under 100mW power dissipation. This can be verified by examining the biased current readings shown in **Table IV**. A quick calculation of power dissipations reveals that each of the 55 boards is consuming approximately one watt dc and considering there are about 18 devices per board, the average power dissipation per part is about 50 milliwatts. Most of the CMOS digital devices were below the 50 mW level, whereas the analog parts were in the 100mW range.

HAST reliability assessment

Since moisture and temperature were the accelerated conditions for this test, Peck's model will again be used as the reliability assessment model. However, since the failure mechanisms are further accelerated due to the biased operating conditions, the model will be used to estimate the total operating hours for the avionics platform in the actual using environment over an expected 20 year lifetime, as described in section IV-A. For this example, a typical circuit board-level operating temperature of +74°C and a humidity level of 80% RH will be assumed:

Again, using equation (3) to calculate the acceleration factor:

$$A.F. = (0.80)^3 \exp(Ea/K*347) / (0.85)^3 \exp(Ea/K*398) = 56.4$$

Factoring the 240 hour test duration by this acceleration factor, this equates to:

$$(240 \text{ test hours}) * (56.4) = 13,536 \text{ equivalent operating hours.}$$

Since the expected operating hours for the avionics system over a 20 year period are 8,000 flight + 4,800 ground = 12,800 hours, the predicted lifetime is:

(13,536 equivalent op hours / 12,800 expected op hours) * 20

= 21 years

VII. Comments

The testing for this experiment was performed in a serial sequence (see Figure 2. test plan). Consequently, the boards were subjected to the cumulative environments of extended burn-in, temperature, cycle, autoclave and HAST.

From a conservative point of view, and not knowing the cumulative effect associated with the interactions of each test, all interactions were ignored and the reliability assessment for each accelerated test environment was evaluated separately.

Also, since the purpose of the testing was not to establish mean time between failures (MTBFs); the tests were not carried to a median failure point. Instead, for the given sample sizes (40-69) the testing was conducted until the predicted life for a given accelerated environment attained the duration required for the using environment (in this case 20 yrs). The stipulation was that all tested devices must pass the required tests. Thus, if a failure occurred in a given accelerated test and it was attributable to a failure mechanism of that test, then that particular device would be unacceptable for the corresponding using environment of the intended application.

Most of the damage observed during the course of the testing was to printed circuit boards, solder connections and the support bias components, not the actual microcircuits. This was primarily due to the fact that the accelerated environments selected to test the microcircuits were excessive for the PWBs and the solder interconnections. Many of the suppliers of HAST and autoclave equipment, as well as testing facilities, recommend testing microcircuits using socketed boards with solderless connections to avoid potential contamination by soldered connections. This, in fact, is the preferred approach a company should take to support an ongoing test program that plans to use PEMs in their future designs. The test carriers are reusable, more survivable and introduce fewer

contaminants. The down side is that one must insure that devices receive the proper preconditioning in the form of time/ temperature exposures that reflect the eventual solder reflow profiles that will be seen in manufacturing.

VIII. Conclusions

The primary purpose of this testing was to obtain experimental data that would evaluate long term survivability of surface-mount PEM microcircuits for a specific military avionics application.

Most of the microcircuits tested exhibited no failures through the environmental test sequence performed. There were 7 devices failures out of 1248 and all 7 were submitted for failure analysis to understand the failure mechanisms involved.

In general, the test results support the justification for the use of plastic encapsulated device types for an application that had previously been limited to traditional ceramic, military part types. We conclude that the surface-mount plastic encapsulated microcircuits we selected, which passed, can be used in the avionics environment described herein.

For the devices exhibiting failures, alternate choices have been made. The final analysis for these failures is still ongoing and additional results are expected in the future.

Of greater significance is the fact that this testing only represents an initial qualification effort designed to validate the feasibility of using specific, commercially available plastic encapsulated microcircuits for a specific military avionics application. In order to utilize existing commercial / industrial technology for future military avionics applications, a continued effort must be made to evaluate each new part type for each application. Ultimately, part qualification and reliability data should be obtained from part manufacturers. However, if this data is not available or not adequate, then accelerated tests similar to the ones presented here are recommended.

IX. Acknowledgment

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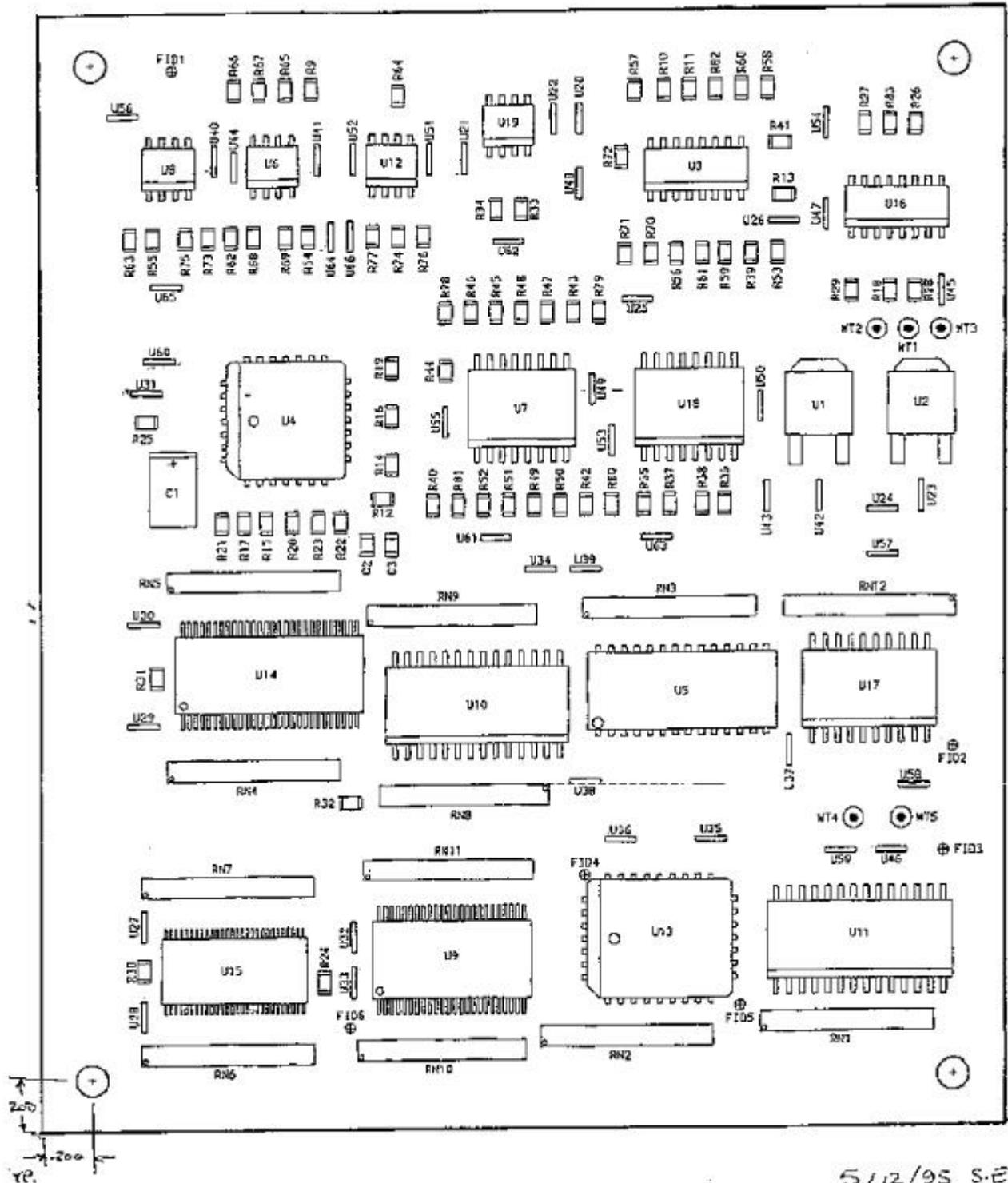


Figure 1. Test Circuit Board Layout

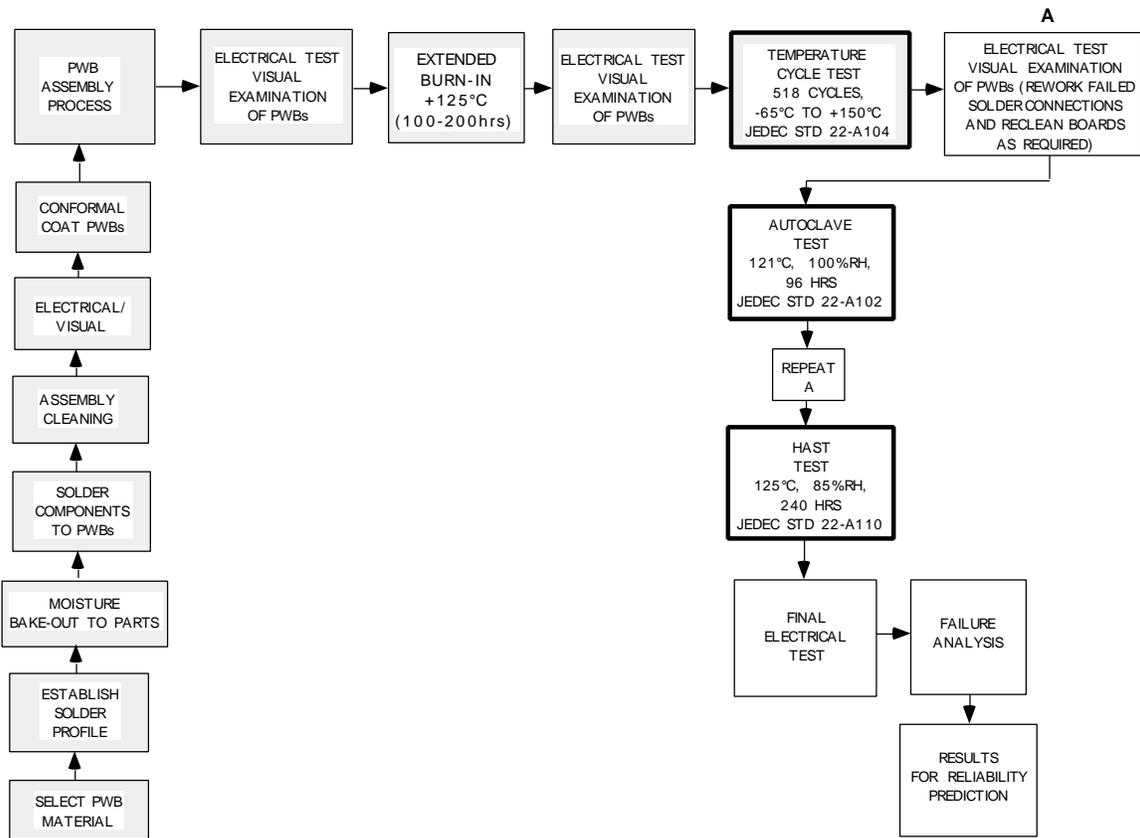
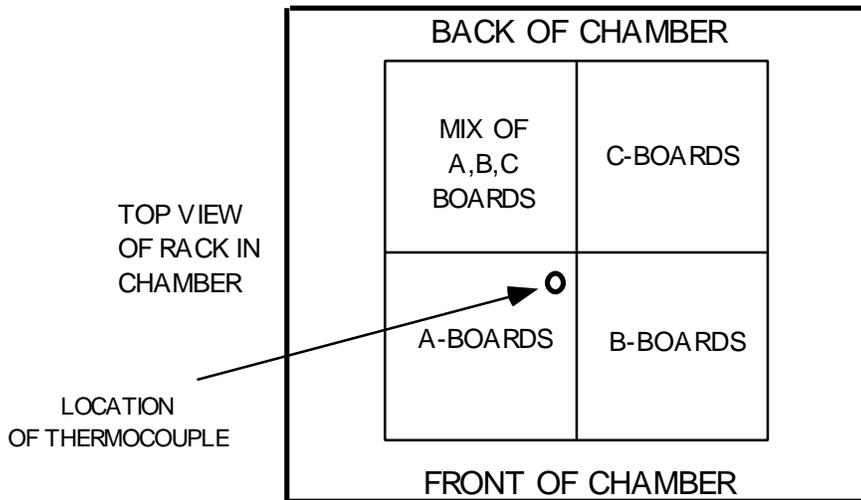


Figure 2. Test Plan



SIDE VIEW OF RACK COLUMNS
(showing board locations by serial number)

	A	B	C	MIX
1	1	1	1	18A
2	2	2	2	19A
3	3	3	4	20A
4	4	4	5	21A
5	5	5	6	22A
6	6	6	8	17B
8	7	7	9	18B
9	8	8	10	19B
10	9	9	11	22B
11	10	10	12	23B
12	11	11	13	19C
13	12	12	14	20C
14	13	13	15	21C
15	14	14	16	22C
16	15	15	17	23C
17	16	16	18	(empty)
(empty)	(empty)	(empty)	(empty)	(empty)
(empty)	(empty)	(empty)	(empty)	(empty)
(empty)	(empty)	(empty)	(empty)	(empty)
(empty)	(empty)	(empty)	(empty)	(empty)

HORIZONTAL AIR CIRCULATION IN CHAMBER

(FRONT OF RACK) (BACK OF RACK)

Figure 3. Test Board Locations in Temperature Cycle Chamber

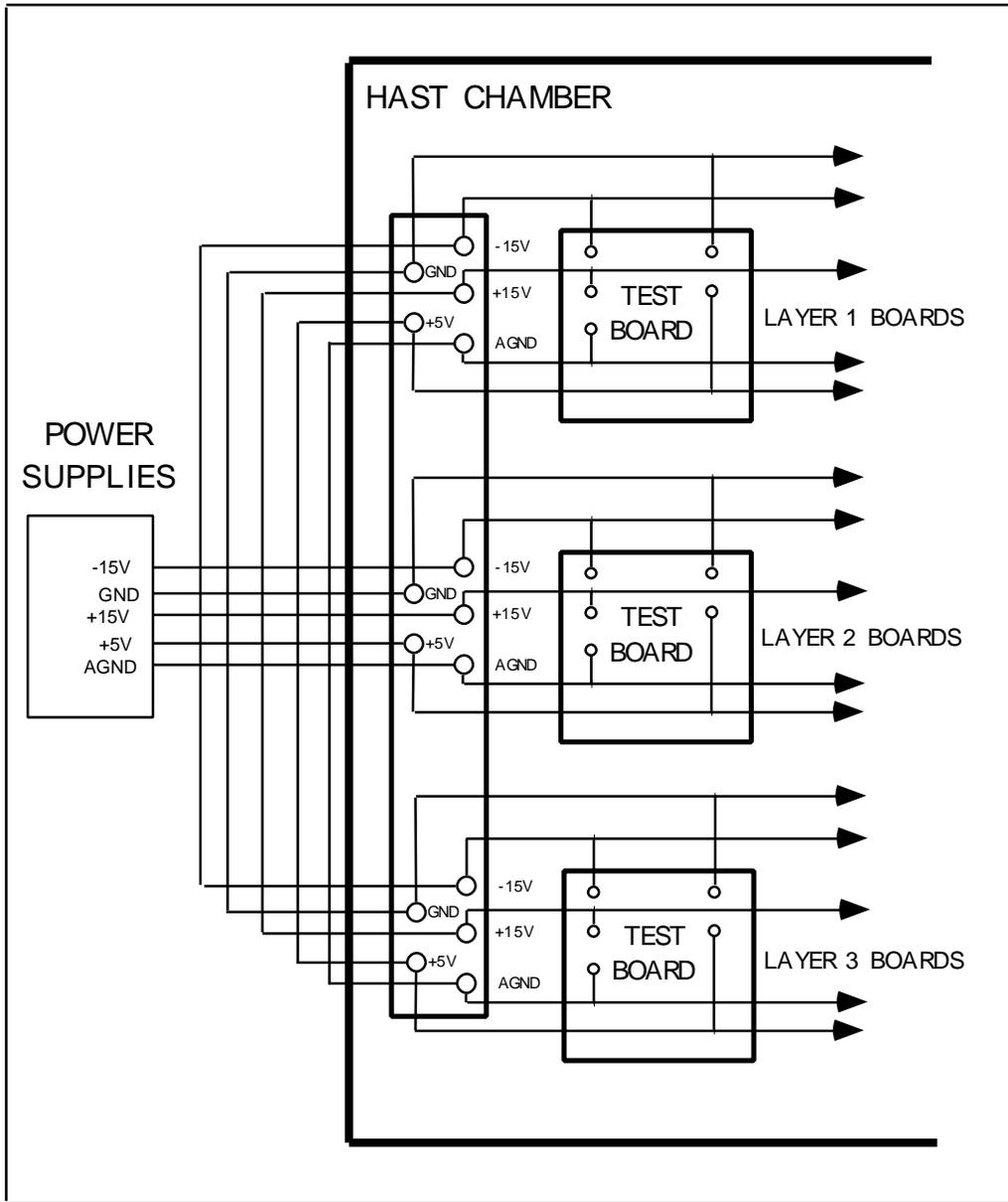


Figure 4.
HAST Biasing Configuration of Test Boards

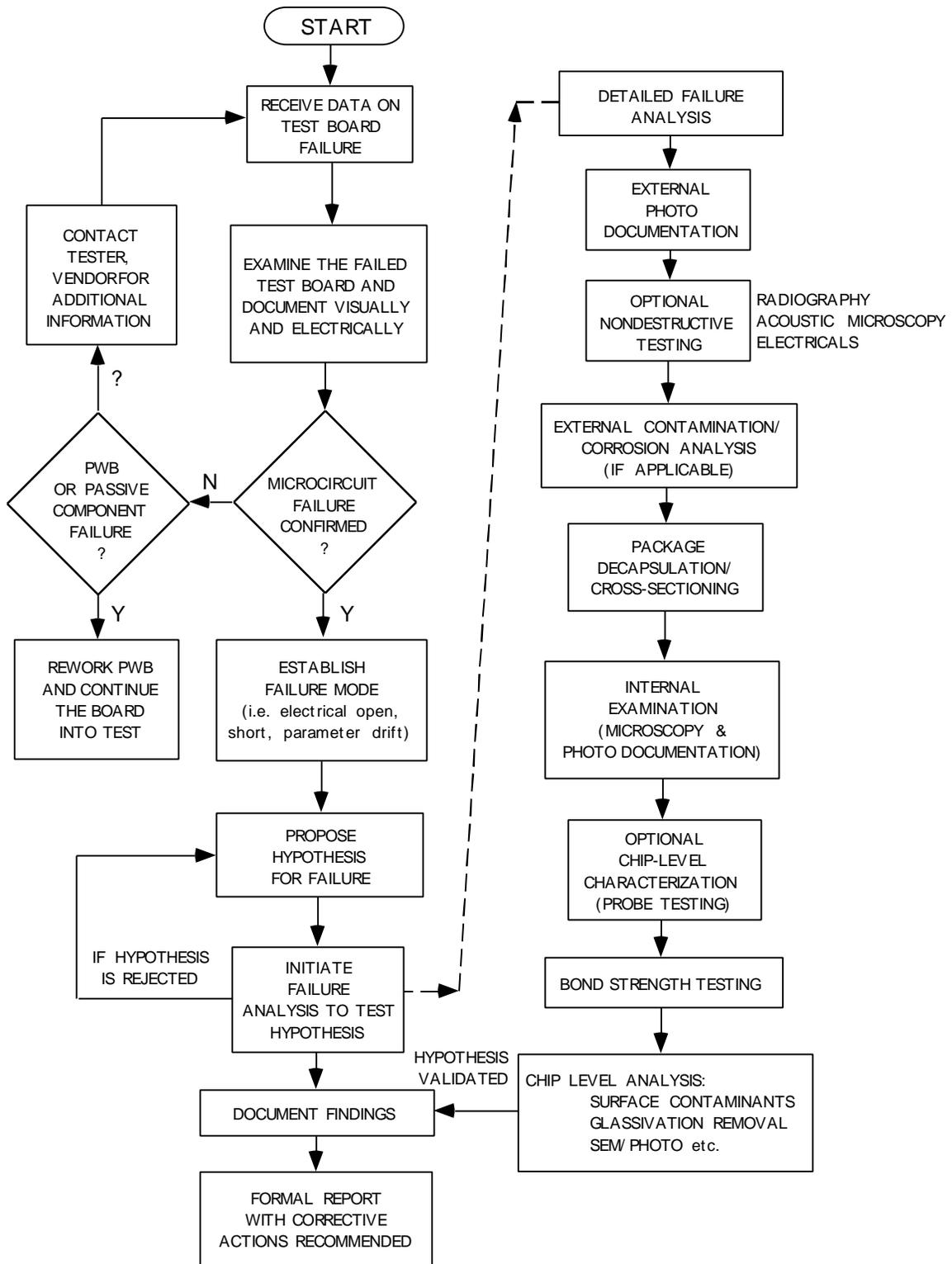


Figure 5. Failure Analysis Plan

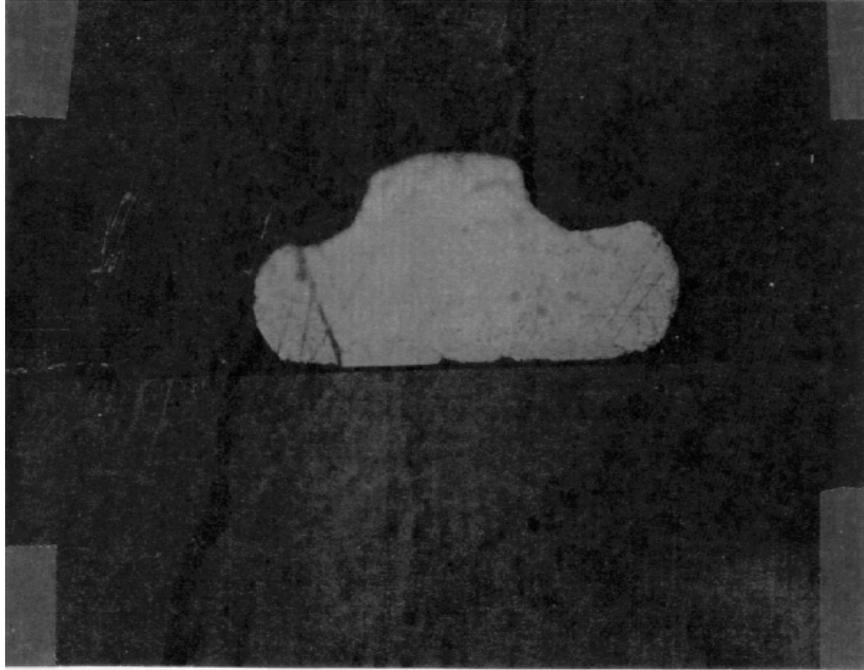


Figure 6
Photomicrograph of cross-section of wire bond on comparator from board 7c.

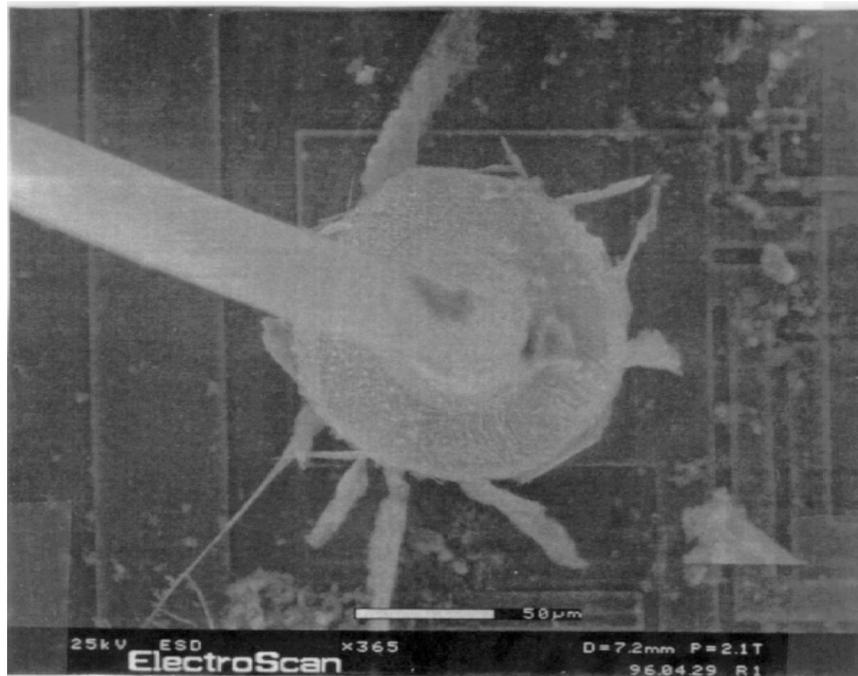


Figure 7
E-SEM photomicrograph of bond pad in comparator from board 5c.



Figure 8
E-SEM photomicrograph of bond pad from 20 bit buffer from board 7c.

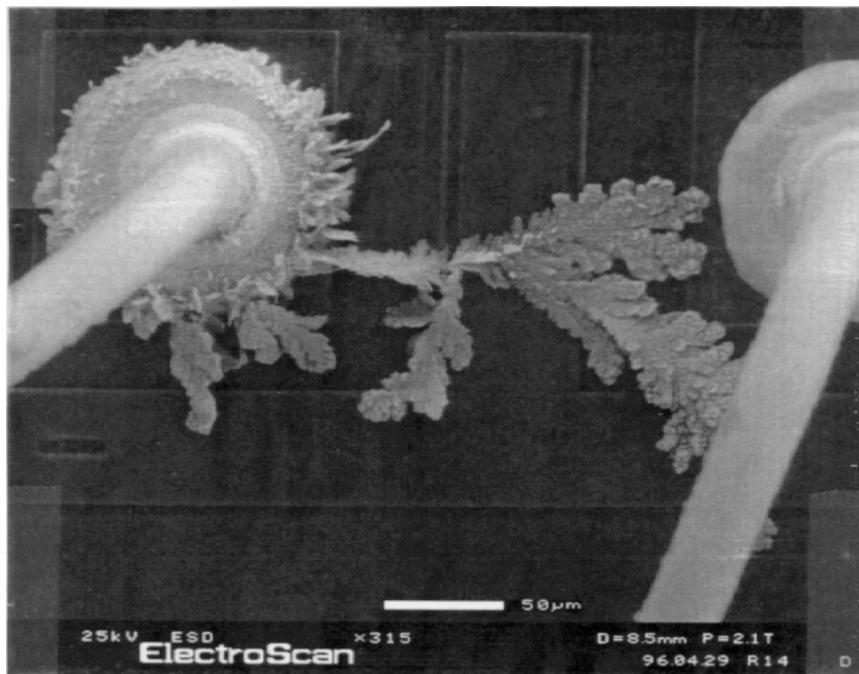


Figure 9
E-SEM photomicrograph of bond pads 5 and 6 on comparator from board 12b.

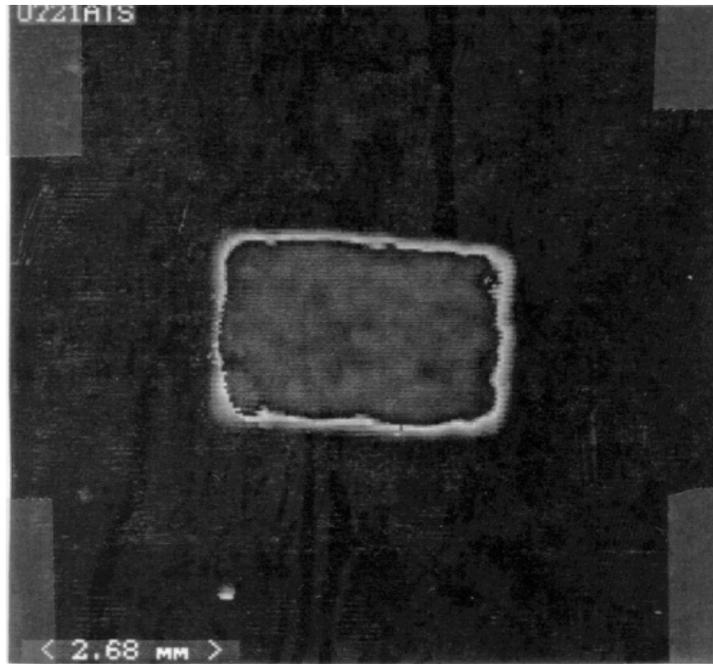


Figure 10
Top of die delamination in quad op-amp which failed after autoclave.

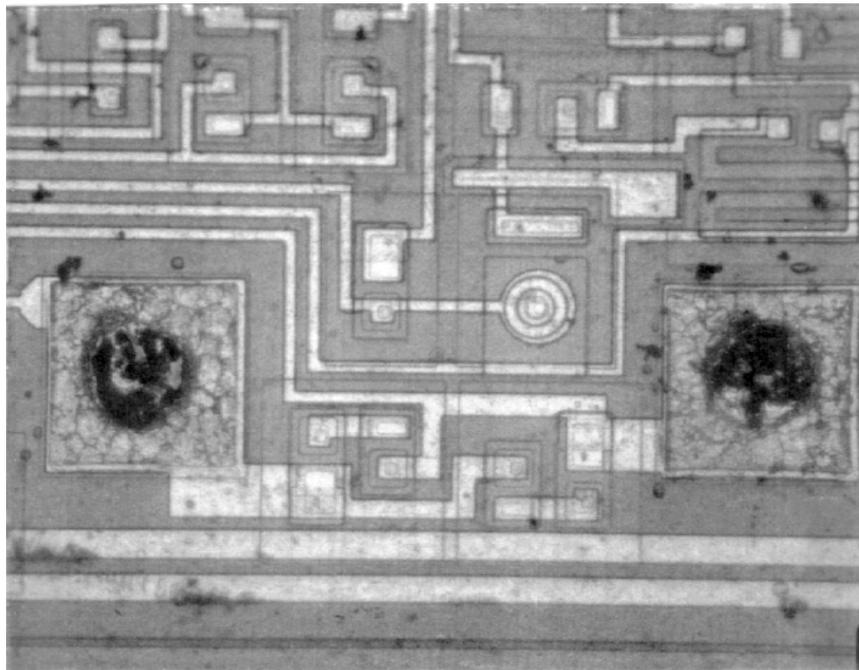


Figure 11
E-SEM photomicrograph of bond pads in quad op-amp failing autoclave.

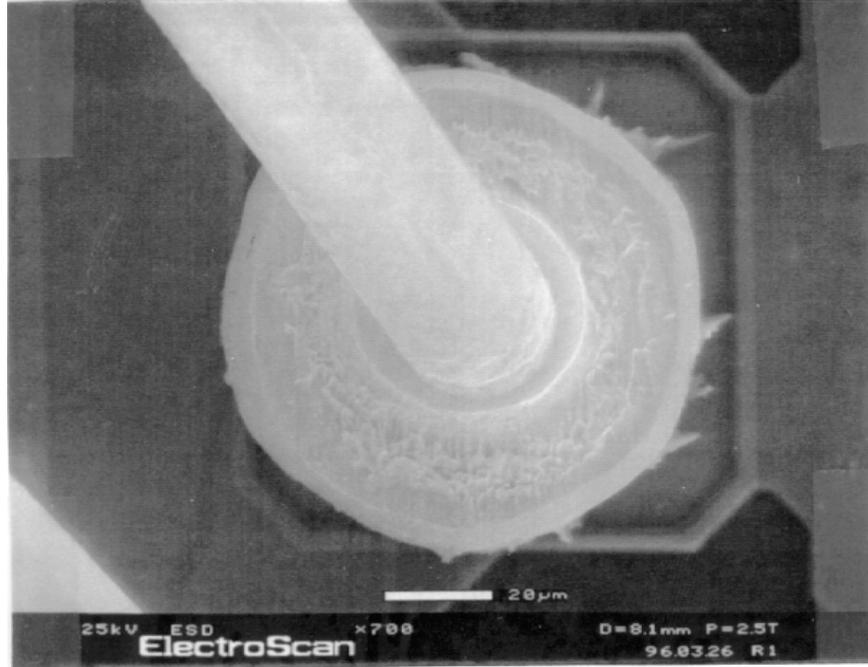


Figure 12
E-SEM photomicrograph of bond pad on 20 bit buffer failing parametrically.

Table I. Selected Microcircuits for Testing

<u>Description</u>	<u>Designator</u>	<u>Package</u>
+12V REGULATOR	U1	FP3
-12V REGULATOR	U2	FP3
QUAD VOLTAGE COMPARATOR	U3	SOP16
PLL CLOCK DRIVER	U4	PLCC28
8K x 8 SRAM	U5	SOJ28
HI TEMP DUAL OP AMP	U6	SOP8
QUAD OP AMP	U7	SOP16
LO NOISE OP AMP	U8	SOP8
16 BIT BUFFER	U9	SSOP48
OCTAL REGISTER	U10	SOP28
8K x8 NVSRAM	U11	SOIC28
OP AMP	U12	SOP8
32K x 8 PROM	U13	PLCC32
SCAN LINE DRIVER TRANSCEIVER	U14	SSOP56
20 BIT BUFFER	U15	TSSOP56
QUAD DIFFERENTIAL DRIVER	U16	SOP16
OCTAL BUS TRANSCEIVER	U17	SOP20
OP AMP	U18	SOP16
COMPARATOR	U19	SOP8

Table II. Summary of Test Results

TEST	NUMBER OF BOARDS INTO TEST	NUMBER OF DEVICES INTO TEST	BOARDS NOT SUBJECTED TO TEST	DEVICE FAILURES FOR ANALYSIS AFTER TEST
STARTING QUANTITIES:	69	1248	–	–
EXTENDED BURN-IN	68	1230	1 ⁽¹⁾	4 ⁽⁶⁾
TEMPERATURE CYCLE	63	1139	5 ⁽²⁾	–
AUTOCLAVE	50	906	13 ⁽³⁾	2 ⁽⁷⁾
HAST (168 hrs)	55	992	8 ⁽⁴⁾	–
HAST (240 hrs)	50	899	5 ⁽⁵⁾	1 ⁽⁸⁾

- (1) 3C held out and designated as control board
- (2) 4 Boards in retest/reclean; 23A held out for salt fog test
- (3) 13 additional Boards in rework for resistor and board via failures
- (4) 8 Boards still in rework for resistor and board via failures
- (5) 5 Boards removed for analysis of low current after 168 hours of HAST
- (6) 3-(U19) Comparators and 1-(U15) 20 bit buffer
- (7) 1-(U15) 20 bit buffer and 1-(U7) Op Amp
- (8) 1-(U19) Comparator

Table III. Accumulated Hours for Extended Burn-in

Burn-in Test Log					
		Elapsed Time (hh:mm)			
Start	Stop	Group A	Group B	Group C	Group D
9/12/95 11:43	9/14/95 9:07	45:24			
9/14/95 17:48	9/20/95 9:00	135:12			
9/20/95 14:20	9/28/95 8:00	185:40			
9/28/95 14:15	9/30/95 14:45	48:30	48:30		
9/30/95 17:00	10/3/95 15:22	70:22	70:22	70:22	
10/3/95 16:10	10/5/95 9:10	41:00	41:00	41:00	41:00
Total time:		526:08	159:52	111:22	41:00

Definitions:

- Group A 4 pilot boards entered test 9/12/95
- Group B 34 Paralene and uncoated boards entered test 9/28/95
- Group C 28 Silicone boards entered test 9/30/95
- Group D 2 final uncoated boards entered test 10/3/95
1 board serial; number 3C; no burn-in (control board)

Table IV.
HAST Test Circuit Board Current Readings

DATE	TIME	-15Vdc (amps)			+15Vdc (amps)			+5Vdc (amps)		
		Layer 1	Layer 2	Layer 3	Layer 1	Layer 2	Layer 3	Layer 1	Layer 2	Layer 3
1/3/96	17:30	0.60	0.60	0.60	0.57	0.59	0.58	0.64	0.84	0.62
1/4/96	11:00	0.58	0.58	0.58	0.54	0.56	0.54	0.61	0.81	0.60
1/4/96	18:00	0.58	0.58	0.58	0.54	0.56	0.54	0.61	0.82	0.61
1/5/96		Steam	Leak;	Valve	Fixed					
1/5/96		0.60	0.60	0.60	0.56	0.58	0.57	0.63	0.83	0.61
1/8/96	10:00	0.61	0.61	0.61	0.57	0.59	0.58	0.63	0.83	0.61
1/8/96	17:30	0.60	0.60	0.60	0.56	0.58	0.57	0.63	0.83	0.61
1/9/96	9:30	0.62	0.62	0.62	0.60	0.62	0.61	0.61	0.81	0.60
1/9/96	18:00	0.62	0.62	0.62	0.60	0.62	0.61	0.60	0.81	0.60
1/10/96	9:00	0.62	0.62	0.62	0.60	0.62	0.61	0.60	0.82	0.60
1/10/96	16:00	0.62	0.62	0.63	0.60	0.60	0.60	0.60	0.82	0.60
1/11/96	8:30	0.62	0.62	0.63	0.60	0.62	0.61	0.60	0.81	0.60
1/11/96	16:30	0.62	0.62	0.62	0.60	0.62	0.61	0.61	0.81	0.60
1/11/96	16:30	Ramp	down	168hrs						
		50	Boards	cont.	test					
1/15/96	14:40	0.49	0.63	0.62	0.46	0.62	0.62	0.44	0.65	0.70
1/16/96	8:45	0.49	0.63	0.63	0.47	0.62	0.62	0.44	0.65	0.70
1/16/96	17:00	0.48	0.63	0.63	0.47	0.62	0.62	0.44	0.66	0.71
1/17/96	9:00	0.48	0.63	0.63	0.47	0.62	0.62	0.44	0.66	0.71
1/17/96	17:00	0.48	0.63	0.63	0.47	0.61	0.61	0.44	0.65	0.71
1/18/96	8:30	0.49	0.64	0.63	0.47	0.62	0.62	0.44	0.66	0.72
1/18/96	19:05	0.48	0.63	0.63	0.47	0.62	0.62	0.43	0.66	0.71
1/19/96	11:00	0.48	0.63	0.63	0.47	0.62	0.62	0.44	0.67	0.70
1/19/96	11:30	Test	Finish							

Table V.

Final Device Electrical Test Summary

PART NUMBER	TOTAL DEVICES IN TEST	GENRAD TESTED GOOD	INDIVIDUALLY TESTED	INDIVIDUALLY TESTED GOOD	FAIL
U1	46	45	1	1	0
U2	69	69	0	0	0
U3	69	69	0	0	0
U4	65	61	4	4	0
U5	69	63	6	6	0
U6	69	69	0	0	0
U7	69	68	1	0	1
U8	69	69	0	0	0
U9	69	44	25	25	0
U10	69	62	7	7	0
U11	63	60	3	3	0
U12	69	69	0	0	0
U13	40	39	1	1	0
U14	69	51	18	18	0
U15	68	48	20	18	2
U16	69	69	0	0	0
U17	69	68	1	1	0
U18	69	69	0	0	0
U19	69	65	4	0	4
	1248	1157	91	84	7

Table VI.
Test conditions for parts that were failure analyzed

Board #	Coating	Failed Parts	Failed After	Burn-in (HTOL)	Temperature Cycle	Autoclave	HAST
2b	None	None	No failures	159 hours at 125°C	518 cycles, -65°C to+150°C	96 hours @ 121°C	None
5a	Silicone	U15	Parametric	111 hours at 125°C	518 cycles, -65°C to+150°C	96 hours @ 121°C	None
5c	None	U19	Burn-in	525 hours at 125°C	518 cycles, -65°C to+150°C	96 hours @ 121°C	None
7c	None	U19,U15	Burn-in	525 hours at 125°C	None	None	125°C,85%RH, 240 hrs.biased
9a	None	None	No failures	40 hours at 125°C	518 cycles, -65°C to+150°C	96 hours @ 121°C	125°C,85%RH, 240 hrs.biased
12b	Parylene	U19	Autoclave	159 hours at 125°C	518 cycles, -65°C to+150°C	96 hours @ 121°C	125°C,85%RH, 240 hrs.biased
13b	None	U19	Burn-in	525 hours at 125°C	518 cycles, -65°C to+150°C	None	125°C,85%RH, 240 hrs.biased
21a	Silicone	U7	Autoclave	111 hours at 125°C	518 cycles, -65°C to+150°C	96 hours @ 121°C	125°C,85%RH, 240 hrs.biased

* Failed parts in bold were the test failures submitted for analysis

^[1] L. Condra, S. O’Rear, T. Freedman, L. Flancia, M. Pecht, D. Barker, “Comparison of Plastic and Hermetic Microcircuits Under Temperature Cycling and Temperature Humidity Bias” *IEEE Transactions on Components, Hybrids, and Manufacturing Technology*, vol. 15, no.5, Oct. 1992, pp. 640- 650.

^[2] P. McCluskey, “Accelerated testing of plastic encapsulated microelectronics for military avionics applications” ERS, Inc., May 1996.